DALLAS SEMICONDUCTOR

www.maxim-ic.com

DS1851
Dual Temperature-Controlled NV Digital-to-Analog Converters

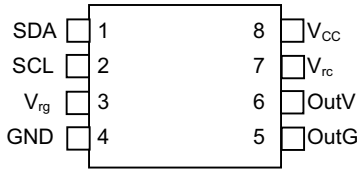
FEATURES

- Two temperature-controlled 8-bit Digital-to-Analog Converters (DACs)
- DAC settings changeable every 4°C
- Access to temperature data and device control through a 2-wire interface
- Operates with +3.3V or +5V supplies
- Packaging: 8-pin TSSOP
- Operating temperature: -40ºC to +95ºC
- Programming temperature: 0ºC to +70ºC

ORDERING INFORMATION

DS1851E-010	8-pin 173mil TSSOP
DS1851E-010/T&R	8-pin Tape and Reel TSSOP

PIN ASSIGNMENTS



8-Pin TSSOP (173mil)

PIN DESCRIPTIONS

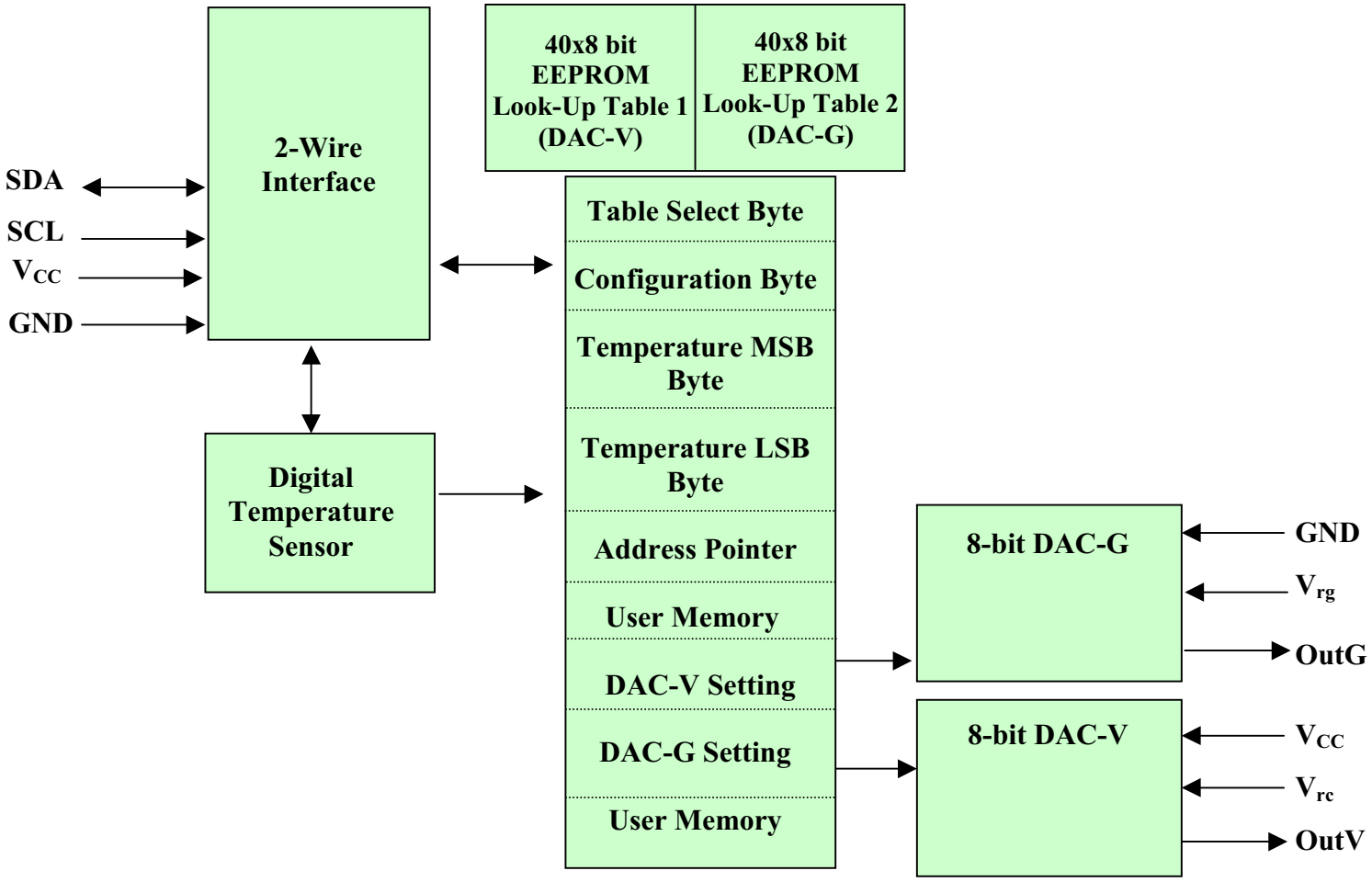
V_{CC}	-	+3.3V or +5V Power Supply Input
GND	-	Ground
SDA	-	2-Wire Serial Data Input/Output
SCL	-	2-Wire Serial Clock Input
OutG	-	DAC Output with Respect to Ground
V_{rg}	-	Reference Input from Ground
OutV	-	DAC Output with Respect to V_{CC}
V_{rc}	-	Reference Input from V_{CC}

DESCRIPTION

The DS1851 dual temperature-controlled nonvolatile (NV) DACs consists of two DACs, two EEPROM look-up tables, and a direct-to-digital temperature sensor. Both of the DACs can be programmed with any temperature coefficient, which means that any system temperature effects can be corrected without any additional external devices. The DS1851 provides an ideal method for setting and temperature-compensating bias voltages and currents in control applications using a minimal amount of external circuitry.

The user-defined settings for both DACs are stored in two EEPROM look-up tables and can be accessed over the industry-standard 2-wire serial bus, which consists of SDA and SCL pins. These look-up tables can assign a unique output value to each DAC for every 4°C increment over the -40°C to +95°C range. The output of the digital temperature sensor is also available as a 12-bit, two's complement value over the serial bus.

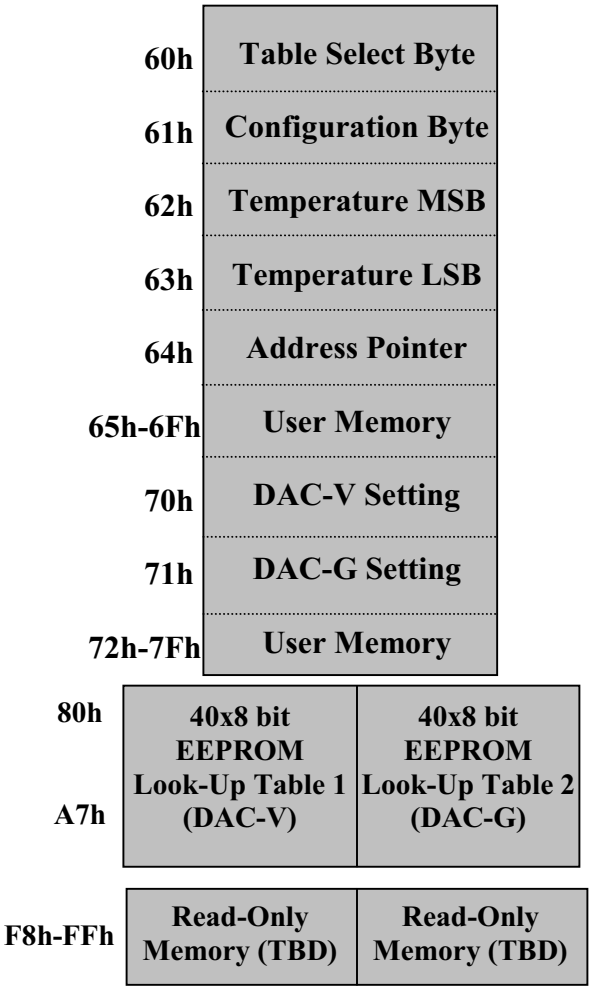
DS1851 BLOCK DIAGRAM Figure 1



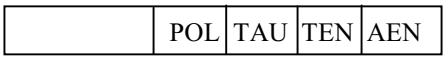
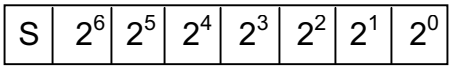
PIN DESCRIPTIONS

Name	Pin	Description
V_{CC}	8	**Power-Supply Terminal.** The DS1851 will support supply voltages ranging from 3.0V to 5.5V.
GND	4	**Ground Terminal**
SDA	1	**2-Wire Serial Data Interface.** The serial data pin is for serial data transfer to and from the DS1851. The pin is open drain and may be wire-OR'ed with other open-drain or open-collector interfaces.
SCL	2	**2-Wire Serial Clock Input.** The serial clock input is used to clock data into the DS1851 on rising edges and clock data out on falling edges.
OutG	5	**DAC-G Output.** This calculated output is between V_{CC} and V_{rg}.
OutV	6	**DAC-V Output.** This calculated output is between V_{CC} and V_{rc}.
V_{rg}	3	**Reference Input from GND.** This input is used for a reference in DAC-G.
V_{rc}	7	**Reference Input from V_{CC}.** This input is used for a reference in the DAC-V.

MEMORY ORGANIZATION



MEMORY LOCATIONS

Memory Location	Name of Location	Function of Location
60h	Table Select Byte	Writing to this byte determines which of the two 40x8 EEPROM look-up tables is selected for reading or writing. 00h (Table 01h selected) 01h (Table 02h selected)
61h	Configuration Byte	 POL — Analog Updating TAU — Temperature/Address Update TEN — Temperature Update Enable AEN — Address Update Enable Default setting is 0Fh, TAU = 1, TEN = 1, and AEN = 1. POL = 1 until power is high enough to guarantee outputs from the analog temperature converter. Once POL = 0, automated updates will begin. TAU becomes a 1 after a temperature and address update has occurred as a result of a temperature conversion. The user can write this bit to 0 and check for a transition from 0 to 1 in order to verify that a conversion has occurred. If TEN = 0, the temperature conversion feature is disabled. The user sets the DAC in manual mode by writing to addresses 70h and 71h to control DAC-V and DAC-G, respectively. With AEN = 0 the user can operate in a test mode. Address updates made from the temperature sensor will cease. The user can load a memory location into 64h and verify that the values in locations 70h and 71h are the expected user-defined values.
62h	Temperature MSB	This byte contains the MSB of the 12-bit 2's complement temperature output from the temperature sensor. 

Memory Location	Name of Location	Function of Location
63h	Temperature LSB	This byte contains the LSB of the 12-bit 2's complement temperature output from the temperature sensor. 2^{-1} | 2^{-2} | 2^{-3} | 2^{-4} | X | X | X | X
64h	Address Pointer	Calculated, current DAC address (80h–A7h). The user-defined DAC setting at this location in the respective look-up table will be loaded into 70h and 71h to set the two DACs.
65h to 6Fh	User Memory	General-purpose user memory
70h	DAC-V Setting	In the user-controlled setting mode, this block contains the DAC-V setting.
71h	DAC-G Setting	In the user-controlled setting mode, this block contains the DAC-G setting.
72h to 7Fh	User Memory	General-purpose user memory
80h to A7h	User-Defined Look-Up Table	This block contains the user-defined temperature settings of the DACs. Values between 00h and FFh can be written to either table to set the 8-bit DACs. The first address location, 80h, is used to set the DAC at -40°C. Each successive memory location will contain the DAC setting for the previous temperature +4°C. For example, memory address 81h is the address that will set the DAC in a -36°C environment.

DAC OPERATION

One DAC performs an 8-bit analog conversion using the difference between V_{rc} and V_{CC} as the reference. The output values follow the following equation:

$$OutV = V_{rc} + (V_{CC} – V_{rc}) * DACreg1/255$$

DACreg1 is the decimal equivalent of the digital value to be converted to analog.

The other DAC performs an 8-bit analog conversion using the difference between V_{rg} and GND as the reference. The output values follow the following equation:

$$OutG = V_{rg} - (V_{rg} – GND) * DACreg2/255$$

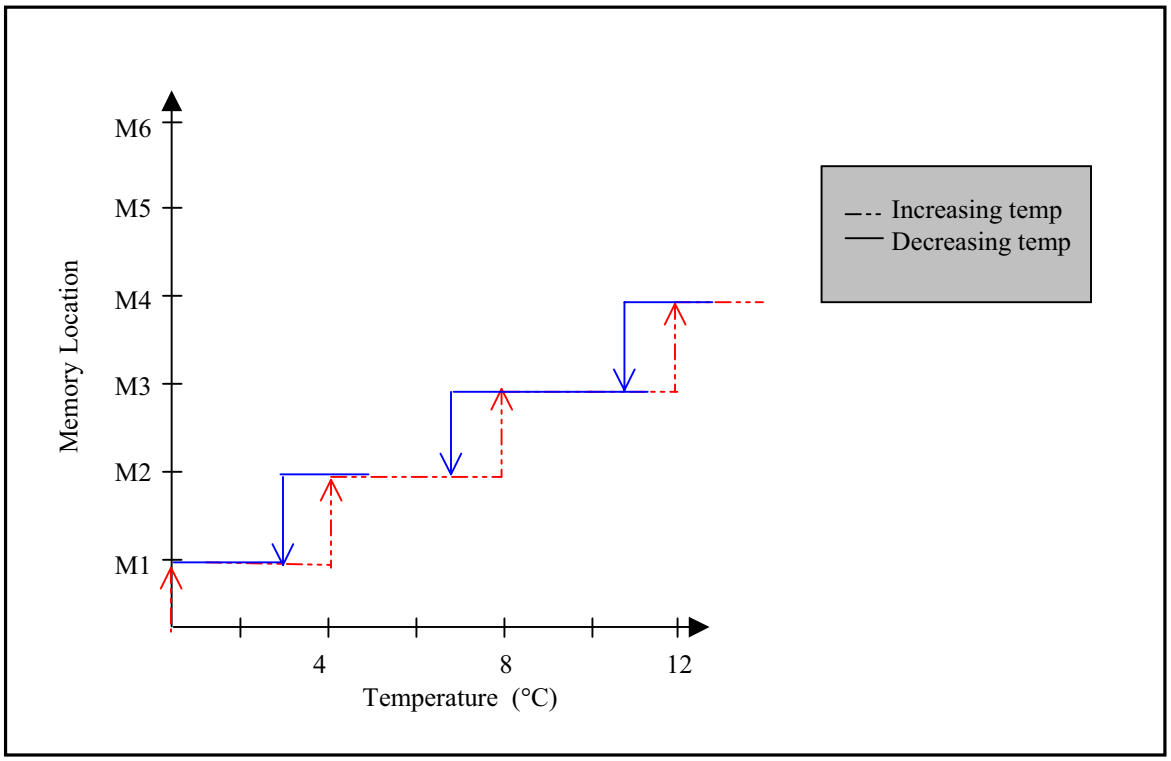
DACreg2 is the decimal equivalent of the digital value to be converted to analog.

TEMPERATURE CONVERSION

The direct-to-digital temperature sensor measures temperature through the use of an on-chip temperature measurement technique with an operating range from -40°C to +95°C. Temperature conversions are initiated upon power-up, and the most recent result is stored in address locations 62h and 63h, which are updated every 10ms. Temperature conversion will not occur during an active read or write to memory.

The values of the DACs are determined by the temperature-addressed look-up table that assigns a unique value to both for every 4°C increment with a 1°C hysteresis at a temperature transition over the operating temperature range. (See Figure 2.)

MEMORY LOCATION OVER TEMPERATURE Figure 2



2-WIRE OPERATION

Clock and Data Transitions

The SDA pin is normally pulled high with an external resistor or device. Data on the SDA pin may only change during SCL low time periods. Data changes during SCL high periods will indicate a START or STOP conditions depending on the conditions discussed below. Refer to the Timing Diagram in Figure 4 for further details.

START Condition

A high-to-low transition of SDA with SCL high is a START condition that must precede any other command. Refer to the timing diagram in Figure 4 for further details.

STOP Condition

A low-to-high transition of SDA with SCL high is a STOP condition. After a read sequence, the stop command places the DS1851 into a low-power mode. Refer to the timing diagram in Figure 4 for further details.

Acknowledge Bit

All address bytes and data bytes are transmitted via a serial protocol. The DS1851 pulls SDA low during the ninth clock pulse to acknowledge that it has received each word.

Standby Mode

The DS1851 features a low-power mode that is automatically enabled after power-on, after a STOP command, and after the completion of all internal operations.

2-Wire Interface Reset

After any interruption in protocol, power loss, or system reset, the following steps reset the DS1851:

1) Clock up to nine cycles.
2) Look for SDA high in each cycle while SCL is high.
3) Create a START condition while SDA is high.

Device Addressing

The DS1851 must receive an 8-bit device address word following a START condition to enable a specific device for a read or write operation. The address word is clocked into the DS1851 MSB to LSB. The address word consists of Ah (1010) followed by 000 then the R/W bit. If the R/W bit is high, a read operation is initiated. The R/W is low, a write operation is initiated. Upon a match of the address, the DS1851 will output a zero for one clock cycle as an acknowledge. If the address does not match, the DS1851 ignores the communication.

Write Operations

After receiving a matching address byte with the R/W bit set low, the device goes into the write mode of operation. The master must transmit an 8-bit EEPROM memory address to the device to define the address where the data is to be written. After the byte has been received, the DS1851 will transmit a zero for one clock cycle to acknowledge the receipt of the address. The master must then transmit an 8-bit data word to be written into this address. The DS1851 will again transmit a zero for one clock cycle to acknowledge the receipt of the data. At this point, the master must terminate the write operation with a stop condition. The DS1851 then enters an internally-timed write process T_w to the EEPROM memory. All inputs are disabled during this byte write cycle.

The DS1851 is capable of an 8-byte page write. A page write is initiated the same way as a byte write, but the master does not send a STOP condition after the first byte. Instead, after the slave acknowledges receipt of the data byte, the master can send up to seven more bytes using the same nine-clock sequence. The master must terminate the write cycle with a STOP condition or the data clocked into the DS1851 will not be latched into permanent memory.

Acknowledge Polling

Once the internally-timed write has started and the DS1851 inputs are disabled, acknowledge polling can be initiated. The process involves transmitting a START condition followed by the device address. The R/W bit signifies the type of operation that is desired. The read or write sequence will only be allowed to proceed if the internal write cycle has completed and the DS1851 responds with a zero.

Read Operations

After receiving a matching address byte with the R/W bit set high, the device goes into the read mode of operation. There are three read operations: current address read, random read, and sequential address read.

Current Address Read

The DS1851 has an internal address register that contains the address used during the last read or write operation, incremented by one. This data is maintained as long as V_{CC} is valid. If the most recent address was the last byte in memory, then the register resets to the first address. This address stays valid between operations as long as power is available.

Once the device address is clocked in and acknowledged by the DS1851 with the R/W bit set to high, the current address data word is clocked out. The master does not respond with a zero, but does generate a STOP condition afterwards.

Random Read

A random read requires a dummy-byte write-sequence to load in the data word address. Once the device and data address bytes are clocked in by the master and acknowledged by the DS1851, the master must generate another START condition. The master now initiates a current address read by sending the device address with the R/W bit set high. The DS1851 will acknowledge the device address, then serially clocks out the data byte.

Sequential Address Read

Sequential reads are initiated by either a current address read or a random address read. After the master receives the first data byte, the master responds with an acknowledge. As long as the DS1851 receives this acknowledge after a byte is read, the master may clock out additional data words from the DS1851. After reaching address FFh, it resets to address 00h.

The sequential read operation is terminated when the master initiates a STOP condition. The master does not respond with a zero.

2-WIRE SERIAL PORT OPERATION

The 2-wire serial port interface supports a bidirectional data transmission protocol with device addressing. A device that sends data on the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master." The devices that are controlled by the master are "slaves." The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1851 operates as a slave on the 2-wire bus. Connections to the bus are made via the open-drain I/O lines, SDA and SCL. The following I/O terminals control the 2-wire serial port: SDA and SCL. Timing diagrams for the 2-wire serial port can be found in Figures 3 and 4. Timing information for the 2-wire serial port is provided in the AC Electrical Characteristics table for 2-wire serial communications.

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain high.

Start data transfer: A change in the state of the data line from high to low while the clock is high defines a START condition.

Stop data transfer: A change in the state of the data line from low to high while the clock line is high defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line can be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Figures 3 and 4 detail how data transfer is accomplished on the 2-wire bus. Depending upon the state of the R/W bit, two types of data transfer are possible.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Within the bus specifications, a regular mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined. The DS1851 works in both modes.

Acknowledge: Each receiving device, when addressed, generates an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end-of-data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the STOP condition.

1) Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the command/control byte, followed by a number of data bytes. The slave returns an acknowledge bit after each received byte.

2) Data transfer from a slave transmitter to a master receiver. The master transmits the first byte (the command/control byte) to the slave. The slave then returns an acknowledge bit. Next, follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a ‘not acknowledge’ can be returned.

The master device generates all serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

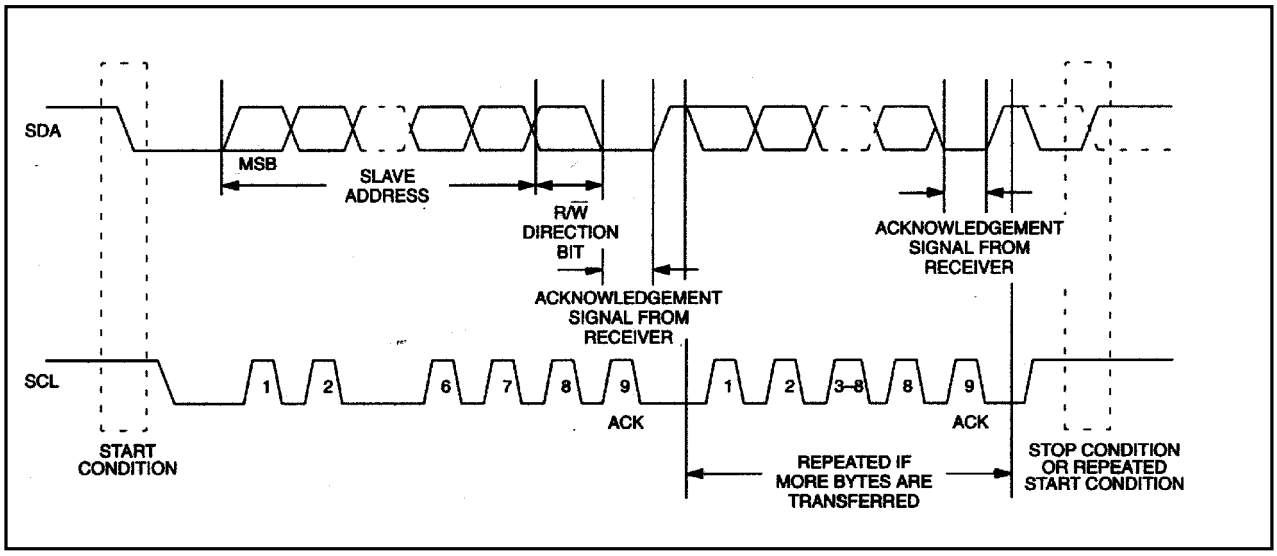
The DS1851 may operate in the following two modes:

1) **Slave receiver mode:** Serial data and clock are received through SDA and SCL respectively. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave (device) address and direction bit.

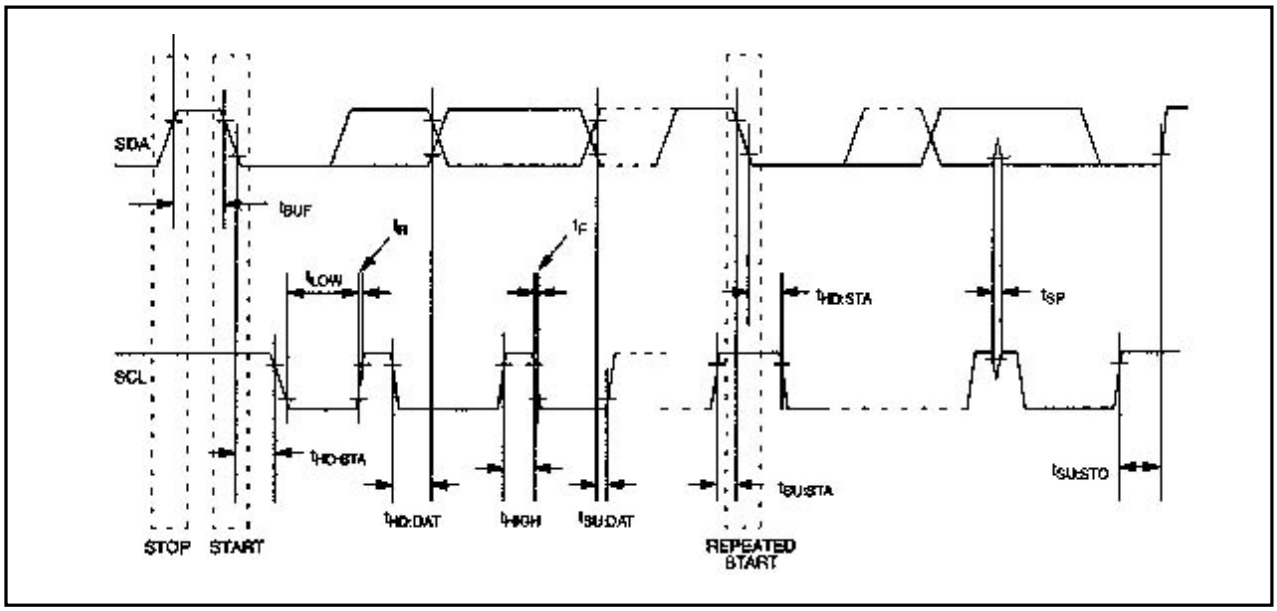
2) **Slave transmitter mode:** The first byte is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1851 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

Following the START condition, the DS1851 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the *1010000* control code and the read/write bit, the slave device outputs an acknowledge signal on the SDA line.

2-WIRE DATA TRANSFER PROTOCOL Figure 3



2-WIRE TIMING DIAGRAM Figure 4



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +6.0V
Operating Case Temperature Range	-40°C to +95°C
Programming Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (-40°C to +95°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	+3.0		+5.5	V	1

DC ELECTRICAL CHARACTERISTICS (-40°C to +95°C; V_{CC} = +3.0V to +5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Active Current	I_{CC}			0.6	1	mA	8
Input Leakage	I_{LI}		-1		+1	µA	
Input Logic 1	V_{IH}		$0.7V_{CC}$		V_{CC} + 0.3	V	
Input Logic 0	V_{IL}		GND - 0.3		$0.3V_{CC}$	V	
Input Current each I/O Pin		$0.4<V_{I/O}<0.9V_{CC}$	-10		+10	µA	
Low-Level Output Voltage (SDA)	V_{OL1}	3mA sink current	0		0.4	V	
	V_{OL2}	6mA sink current	0		0.6	V	

AC ELECTRICAL CHARACTERISTICS (-40°C to +95°C, V_{CC} = 3.0V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
SCL Clock Frequency	f_{SCL}	Fast Mode Standard Mode	0 0		400 100	kHz	6
Bus Free Time Between STOP and START Condition	t_{BUF}	Fast Mode Standard Mode	1.3 4.7			µs	6
Hold Time (repeated) START Condition	$t_{HD:STA}$	Fast Mode Standard Mode	0.6 4.0			µs	4, 6
Low Period of SCL Clock	t_{LOW}	Fast Mode Standard Mode	1.3 4.7			µs	6
High Period of SCL Clock	t_{HIGH}	Fast Mode Standard Mode	0.6 4.0			µs	6
Data Hold Time	$t_{HD:DAT}$	Fast Mode Standard Mode	0 0		0.9	µs	4, 5, 6
Data Setup Time	$t_{SU:DAT}$	Fast Mode Standard Mode	100 250			ns	6
Start Setup Time	$t_{SU:STA}$	Fast Mode Standard Mode	0.6 4.7			µs	6
Rise Time of Both SDA and SCL Signals	t_R	Fast Mode Standard Mode	$20 + 0.1C_B$		300 1000	ns	6
Fall Time of Both SDA and SCL Signals	t_F	Fast Mode Standard Mode	$20 + 0.1C_B$		300 300	ns	6
Setup Time for STOP Condition	$t_{SU:STO}$	Fast Mode Standard Mode	0.6 4.0			µs	
Pulse Width of Spikes that must be Suppressed by the Input Filter	t_{SP}	Fast Mode	0		50	ns	
I/O Capacitance	$C_{I/O}$				10	pF	
Capacitive Load for Each Bus Line	C_B				400	pF	6
EEPROM Write Time	t_W			10	20	ms	7

DAC (-40°C to +95°C; GND + 0.1<OutG, OutV < V_{CC} - 0.1; V_{CC} = +3.0V to +5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Resolution	N		8			bits	
Nonlinearity	V_{INL}				±2	LSB	
Differential Nonlinearity	V_{DNL}				±1	LSB	
Offset	V_{off}	No load	-10		+10	mV	10
Gain Error	V_{gain}		-0.8		+0.8	%	10, 11
Load Regulation		Source/sink 150µA	-10		+10	mV	
Output Voltage Time Constant	τ			64		µS	
R_{in} at V_{rc} and V_{rg}	R_{in}		22	28	35	kΩ	
C_{load} (OutV/OutG)	C_L				1000	pF	
I_{out} (source/sink, Pin OutV/OutG)	I_{out}				150	µA	
V_{rc} Range	V_{ref}		GND		V_{CC} - 0.5	V	
V_{rg} Range	V_{ref}		GND + 0.5		V_{CC}	V	

DIRECT-TO-DIGITAL TEMPERATURE SENSOR

PARAMETER	SYMBOL	CONDITION	TYP	MAX	UNITS	NOTES
Thermometer Absolute Error	T_{ERR}	-40°C to +95°C		±3	°C	
Conversion Time	t_{CONVT}	12-bit conversion		10	ms	

NOTES:

1. All voltages are referenced to ground.
2. A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} > 250ns$ must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU:DAT} = 1000 + 250 = 1250ns$ before the SCL line is released.
3. After this period, the first clock pulse is generated.
4. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
5. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $VI_{H\ MIN}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
6. C_B - total capacitance of one bus line in pF, timing referenced to $(0.9)(V_{CC})$ and $(0.1)(V_{CC})$.
7. EEPROM-write begins after a STOP condition occurs.
8. Measured with SDA = SCL = $V_{rc} = V_{CC}$, and V_{rg} = GND. The outputs OutV and OutG are left open.
9. Valid at 25°C only.
10. With $V_{rc} = V_{CC}$ -1.25 and V_{rg} = 1.25 + GND.
11. 0.8% is equivalent to 2 LSB.